Amendments to the Claims:

Claim 1 has been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently amended) A method for packaging a flip-chip semiconductor assembly, comprising:

providing at least one integrated circuit (IC) die having bond pads on a surface thereof;

providing a substrate having electrical pads for mounting the at least one IC die thereto;

placing dry conductive epoxy dots on the electrical pads on the substrate;

attaching the at least one IC die to the substrate with the bond pads of the at least one IC die in contact with the dry conductive epoxy dots on the electrical pads on the substrate to form the flip-chip semiconductor assembly with the dry conductive epoxy dots forming an electrical interface therebetween;

electrically testing the flip-chip semiconductor assembly through the electrical interface of the dry conductive epoxy dots;

if the flip-chip semiconductor assembly fails testing, then reworking the flip-chip semiconductor assembly and retesting the flip-chip semiconductor assembly or scrapping the flip-chip semiconductor assembly if the flip-chip semiconductor assembly has already been reworked a preset number of times; and

if the flip-chip semiconductor assembly passes testing, then encapsulating the at least one IC die on the substrate.

2. (Previously presented) The method of claim 1, wherein providing the substrate comprises providing a printed circuit board (PCB).

3. (Previously presented) The method of claim 1, wherein placing the dry conductive epoxy dots comprises placing thermoplastic epoxy and further comprising heating the thermoplastic epoxy followed by cooling the flip-chip semiconductor assembly.

4. (Previously presented) The method of claim 1, wherein attaching the at least one IC die to the substrate comprises:

aligning the bond pads on the at least one IC die with the dry conductive epoxy dots on the electrical pads on the substrate;

contacting the aligned bond pads on the at least one IC die with the dry conductive epoxy dots on the substrate; and

heating the flip-chip semiconductor assembly to form electrical connections between the bond pads on the at least one IC die and the electrical pads on the substrate.

5. (Previously presented) The method of claim 1, further comprising speed grading the at least one IC die.

6. (Previously presented) The method of claim 5, wherein speed grading is performed after testing the flip-chip semiconductor assembly.